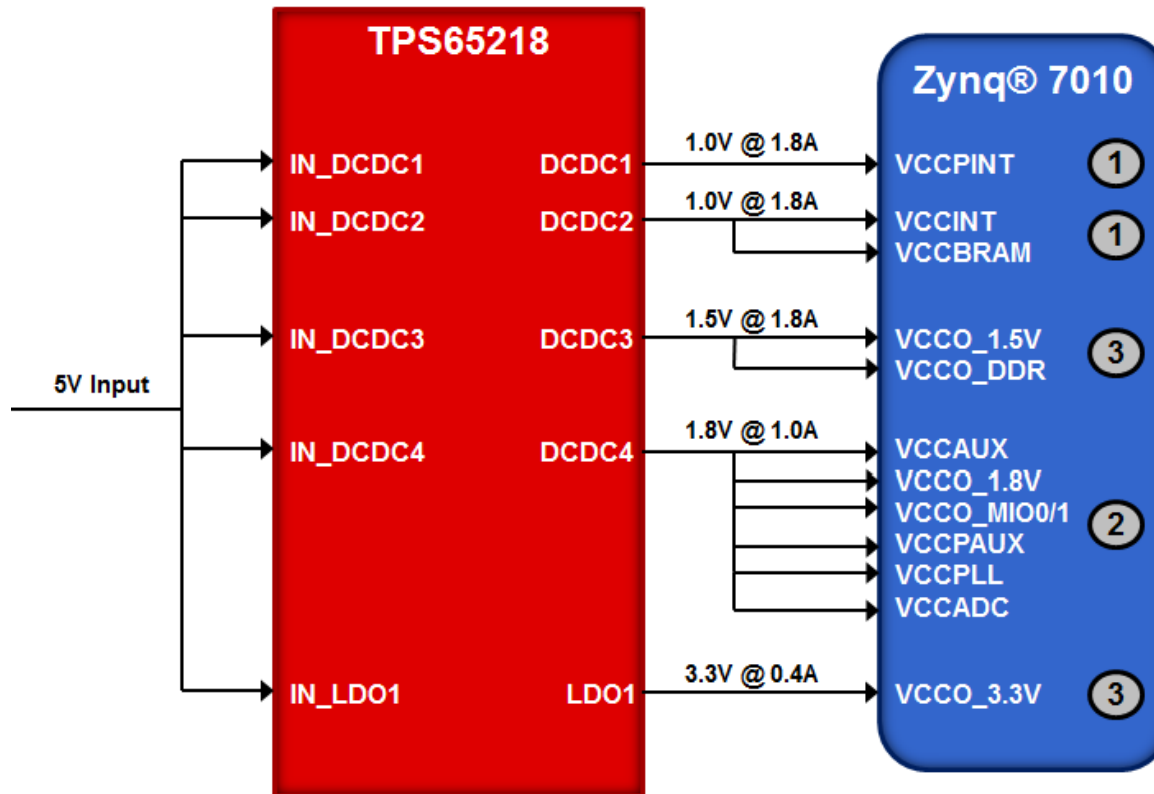


Xilinx® Zynq® 7010 TPS65218 Block Diagram



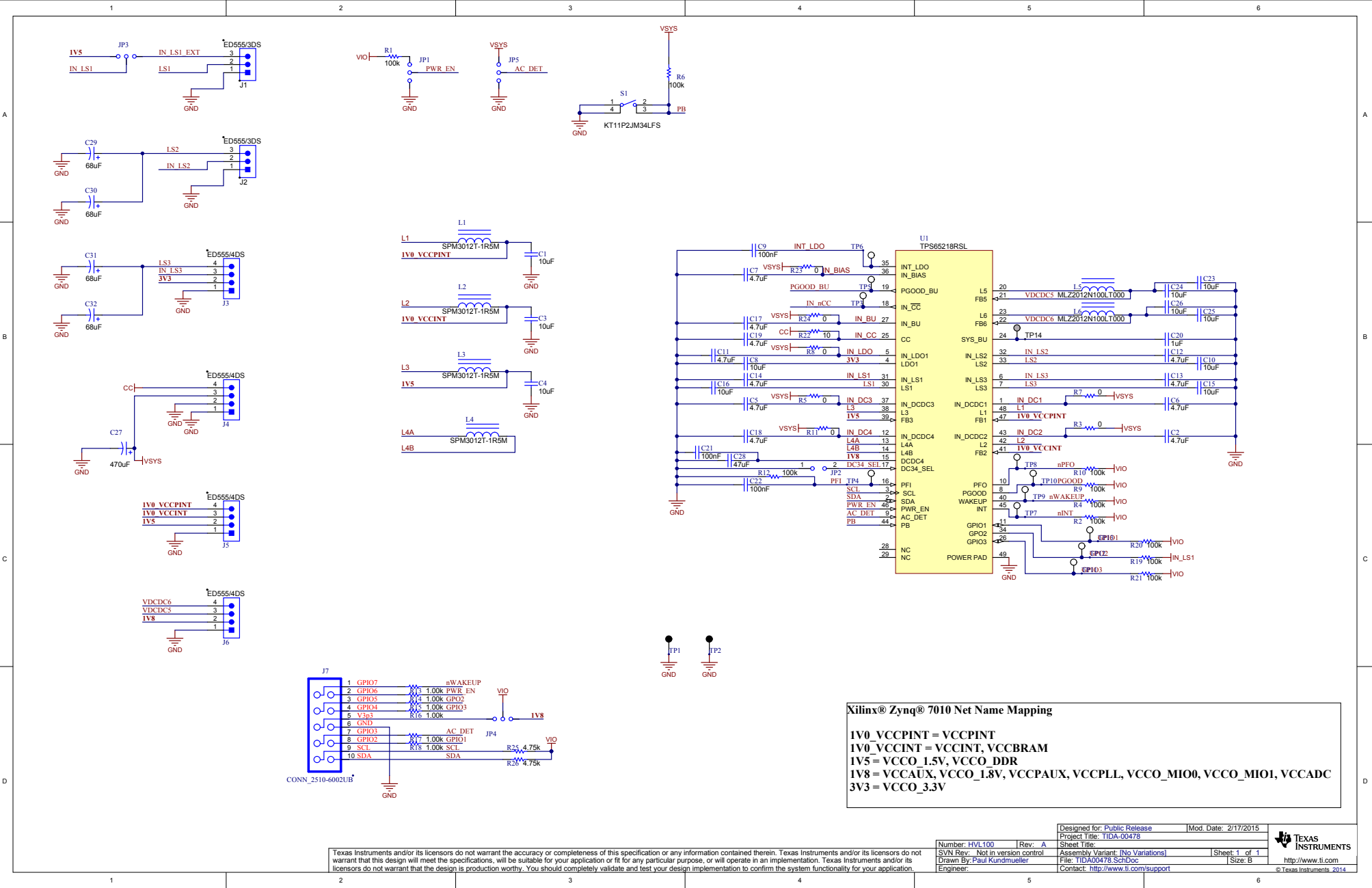
Note:

ⓧ = Power Sequence Order

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Designed for: Public Release		Mod. Date: 2/17/2015	
Project Title: TIDA-00478			
Number: HVL100	Rev: A	Sheet Title: TIDA-00478	Sheet 1 of 1
SUN Rev: Not in version control		Assembly Variant: [No Variations]	
Drawn By: Paul Kundmueller		File: TPS65218_Zynq_7010_Block_Diagram_SchDoc Size: B	
Engineer:		Contact: http://www.ti.com/support	

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Xilinx® Zynq® 7010 Net Name Mapping

IV0_VCCPINT = VCCPINT
IV0_VCCINT = VCCINT, VCCBRAM
IV5 = VCCO_1.5V, VCCO_DDR
IV8 = VCCAUX, VCCO_1.8V, VCCPAUX, VCCPLL, VCCO_MIO0, VCCO_MIO1, VCCADC
3V3 = VCCO_3.3V

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SVN Rev: Not in version control	Assembly Variant: [No Variations]	Project Title: TIDA-00478	Sheet Title:
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